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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,022	07/08/2003	Akira Matsumura	67161-032	9498

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 08/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,022	MATSUMURA, AKIRA	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/8/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1 is rejected under 35 U.S.C. 102(e) as being anticipated by McClure (US Pat. No. 6,709,945 B2).

Regarding claim 1, McClure teaches a manufacturing method of a semiconductor device, comprising the steps of:

forming an insulating film (24) above a semiconductor substrate (10) (see fig. 9);

forming, on said insulating film, a hard mask (92) harder to polish than said insulating film upon chemical mechanical polishing ("CMP") and having a greater selective ratio with respect to said insulating film than a resist film (94) under a prescribed etching condition (see fig. 9 and col. 5, lines 24 and 27-30);

forming a hole ("container") penetrating said hard mask and said insulating film to extend in a vertical direction with respect to a main surface of said semiconductor substrate (see col. 4, lines 55-63);

forming a capacitor lower electrode (100) along a side surface of said hole (see fig. 11);

forming a capacitor dielectric film (110) along a surface of said capacitor lower electrode (see fig. 11); and

forming a capacitor upper electrode (112) to contact a surface of said capacitor dielectric film (see fig. 11).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai (US Pat. No. 5,763,306) in view of McClure (US Pat. No. 6,709,945 B2).

Regarding claim 2, Tsai teaches a manufacturing method of a semiconductor device, comprising the steps of:

forming a first insulating film (12) above a semiconductor substrate (1) (see fig. 4A);

forming, on said first insulating film, a second insulating film (13) (see fig. 4A) different in composition from said first insulating film (please note that layer 12 is an oxide layer and layer 13 is a nitride layer. See col. 5, lines 1-3 and 8-10);

forming, on said second insulating film, a hard mask (14) (see fig. 4A) same in composition with said first insulating film and harder to polish than said second

insulating film upon chemical mechanical polishing (please note that layers 12 and 14 are oxide layers. See col. 5, lines 1-3 and 12-15);

forming, on said hard mask, an etching stopper film (15) (see fig. 4A) having a greater selective ratio than said hard mask under a prescribed etching condition (please note that layer 15 is a polysilicon layer. See col. 5, lines 17-18);

forming, by etching with said etching stopper film used as a mask, a hole (17a) penetrating said etching stopper film (15), said hard mask (14), said second insulating film (13) and said first insulating film (12) to extend in a vertical direction with respect to a main surface of said semiconductor substrate (see fig. 5A);

forming a film to be a capacitor lower electrode (19, 20) on a side surface of said hole and an upper surface of said hard mask (see fig. 8A);

forming a buried film (21) to bury said film to be the capacitor lower electrode (see fig. 9A and col. 6, lines 28-30);

forming the capacitor lower electrode (19, 20) by removing said film to be the capacitor lower electrode (19, 20) and said etching stopper film (15) by chemical mechanical polishing to expose said hard mask (14) (see fig. 9A and col.6, lines 33-36;

forming a capacitor dielectric film (21) on a surface of said capacitor lower electrode (see col. 6, lines 54-55); and

forming a capacitor upper electrode (22) on a surface of said capacitor dielectric film (see fig. 11A).

However, Tsai fails to teach the step of removing the buried film by CMP to expose the hard mask. McClure teaches that it is well known in the art form a buried film

(102) on the capacitor lower electrode (100) (see fig. 10) and remove the buried film (102) and the capacitor electrode (100) by CMP to expose the hard mask (92) (see col. 5, lines 20-26).

Tsai and McClure are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to cover the capacitor lower electrode with a buried film and to remove the buried film by CMP to expose the hard mask. The motivation for doing so, as is taught by McClure, is preventing over-polishing of the underlying films (col. 5, lines 21-30). Therefore, it would have been obvious to combine McClure with Tsai to obtain the invention of claims 2-3.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al. (US Pat. No. 6,656,789 B2) discloses a nitride layer (29), oxide layer (31), a polysilicon layer and an anti-reflection layer (see fig. 5 and col. 6, lines 16-37); Walker (US Pat. No. 5,518,948) discloses a first etch stop (17), oxide (18) and a second etch stop (19) (see fig. 5); Lou (US Pat. No. 6,417,066 B1) discloses a silicon nitride layer 9, an oxide layer (12) and a silicon nitride layer (13) (see fig. 4); and Chen et al. (US Pat. No. 6,190,962 B1) discloses a silicon nitride layer (310), an oxide layer (312) and a silicon nitride layer (314) (see fig. 3E).

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD
8/23/04

Tom Thomas

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